Electronic Version
Stylesheet Version v1.1.1

HIGH RESOLUTION PHASE LOCKED LOOP

Abstract

A phase locked loop (PLL) generates a phase locked signal and adjusts a frequency of the phase locked signal according to an incoming signal. The PLL includes an oscillator for generating the phased locked signal and a frequency detection module electrically coupled to the oscillator. The frequency detection module includes a pattern detector for detecting the two regular patterns in the incoming signal, a counter electrically coupled to the pattern detector for calculating the number of periods of the phase locked signal corresponding to the distance between the two regular patterns, and a comparator electrically coupled to the counter for comparing the number of periods with a predetermined value to generate a control signal, and using the control signal to control the oscillator to adjust the frequency of the phase locked loop signal.